

SEP 29 2008 (General shoulds if necessary)

Application Number:

10/613, 607

Kuo-Reay Peng et al.

07/03/03

Group 11 Univ

PATENT & TRADE MARK OFFICE

[illegible]

FOREIGN PATENT DOCUMENTS

[illegible]

OTHER DOCUMENTS (Including Author, Title, Date, Portion Pages, Etc.)

ML	-	Wu et al., "ESD Protection for Output Pad with Well-Coupled Field-Oxide Device in 0.5 μ m CMOS Technology," IEEE Trans. on Electron Devices, Vol. 44, No. 3, March 1997, IEEE.
ML	-	Ker et al., "ESD Protection Design on Analog Pin with Very Low Input Capacitance for High-Frequency or Current-Mode Applications," IEEE Journal of Solid-State Circuits, Vol. 35, No. 8, Aug.

2000, IEEE -

DATE COMPLETED

6/11/04

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant

SEP 29 1983

Agreement Number

10/613, 607

Kuo-Beang Peng et al.

07/03/03

Order in Unit

~~EXCLUDED
FROM TRADE~~

DATE

NAME _____

مجلس

WOCLES

ΛΥΜΟ ΟΛΤΖ
Ε ΑΡΤΕΡΟΜΥΛΙΣ

DOCUMENT NUMBER

DATE

COUNTRY

CLAS

SUBCLASS

Translation

Y6

32

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

MC

Kleveland et al., "Distributed ESD Protection for High-Speed Integrated Circuits," IEEE Electron Device Letters, Vol. 21, No. 8, Aug. 2000, IEEE.

EXHIBIT

DATE COMPLETED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.